Claims

What is claimed is:

1. A power amplifier circuit comprising:

an input port for receiving a RF input signal;

an output port for providing therefrom a RF output signal, the RF output signal being an amplified version of the RF input signal;

a supply voltage input port for receiving a supply voltage;

a controllable current source having an input port for receiving a control signal and an output port for providing of a variable bias current therefrom, the variable bias current based upon the control signal;

a first amplification stage having a first variable gain and for receiving the RF input signal and for providing a first amplified RF signal, the first amplification stage coupled to the controllable current source for receiving the variable bias current therefrom and for having the first variable gain thereof varied in proportion to the variable bias current;

a second amplification stage having a second gain and coupled to the first amplification stage for receiving the first amplified RF signal and coupled to the output port for providing the output signal thereto; and,

a control circuit for generating the control signal for provision to the controllable current source, the control signal for being generated in dependence upon the supply voltage, where for the supply voltage having a first potential the variable bias current provided to the first amplification stage is smaller than for the supply voltage having a second potential that is lower than the first potential.

2. A power amplifier circuit according to claim 1, where at the first potential the second amplification stage is for operating in an approximately linear mode of operation and at the second potential the second amplification stage is for operating in an approximately saturation mode of operation.

3. A power amplifier circuit according to claim 1, wherein the control circuit comprises a supply voltage sensing circuit having a first input port for sensing of a potential of the supply voltage, a second input port for receiving a reference voltage and having an output port for providing a sense signal therefrom, wherein the variable bias current is variable in proportion to the sense signal.

4. A power amplifier circuit according to claim 3, comprising
a first multiplier circuit comprising at least a first input port connected to the supply voltage sense circuit for receiving the sense signal therefrom, a second input port for receiving a first reference current and having an output port for providing a first current therefrom.

5. A power amplifier circuit according to claim 4, comprising a bandgap current reference circuit having a first output port connected to the first multiplier circuit for providing the first reference current and a second output port for providing a second reference current.

6. A power amplifier circuit according to claim 5, comprising a current summing circuit having a first input port connected to the first multiplier circuit for receiving the first multiplier circuit output current therefrom, a second input port connected to bandgap current reference circuit for receiving the second reference current therefrom and an output port for providing a summed current therefrom, the summed current having a portion of the first current therein that is proportional to the sense signal.

7. A power amplifier circuit according to claim 1, comprising a first inter stage matching circuit, the first inter stage matching circuit disposed between the first amplification stage and the second amplification stage for providing of an impedance match therebetween.

8. A power amplifier circuit according to claim 1, comprising:

a first inter stage matching circuit having output ports coupled to the second amplification stage input ports; and,

a switching circuit having input ports coupled to output ports of the first amplification stage and a first set of output ports coupled to input ports of the first inter stage matching circuit, where the first inter stage matching circuit is for providing an impedance match between the first amplification stage, the switching circuit and the second amplification stage.

9. A power amplifier circuit according to claim 8, comprising:

a third amplification stage having input ports and output ports for providing an amplified version of the RF input signal therefrom; and,

a second inter stage matching circuit having output ports coupled to the third amplification stage input ports and having input ports coupled to a second set of output ports of the switching circuit, where the second inter stage matching circuit is for providing an impedance match between the first amplification stage, the switching circuit and the third amplification stage.

10. A power amplifier circuit according to claim 9, wherein the switching circuit is for controllably switching between providing the first amplified RF signal to one of the second amplification stage and the third amplification stage.

11. A power amplifier circuit according to claim 1, wherein the control circuit comprises a ramp circuit, the ramp circuit for generating of a ramp signal in dependence upon which the control signal is generated.

12. A power amplifier circuit according to claim 11, wherein the control circuit comprises an integrating capacitor, the integrating capacitor for operating in conjunction with the ramp circuit for determining a slope of the ramp signal.

13. A power amplifier circuit according to claim 12, wherein the control circuit comprises an enable port, the enable port for receiving of an enable signal for triggering

of the ramp circuit for generating of the ramp signal, the ramp signal for rising from a first voltage level to a second voltage level during a rise time upon receiving a first transition of the enable signal.

14. A power amplifier circuit according to claim 12, wherein the control circuit comprises an enable port, the enable port for receiving of an enable signal for triggering of the ramp circuit for generating of the ramp signal, the ramp signal for falling from a second voltage level to a first voltage level during a fall time upon receiving a second transition of the enable signal.

15. A power amplifier circuit according to claim 1, wherein the power amplifier circuit comprises a temperature sensing circuit for sensing a temperature of a die on which the power amplifier circuit is formed.

16. A power amplifier circuit according to claim 1, wherein the power amplifier circuit is for use in wireless communication applications.

17. A circuit for biasing a power amplifier circuit comprising a first amplification stage and a second amplification stage, the circuit comprising:

a current source comprising:

a current source input port for receiving a control signal, and

an output port for providing a variable bias current in dependence upon the control signal; and,

a current source control circuit comprising:

a supply voltage input port for receiving of a supply voltage,

a control signal output port coupled to the current source input port for providing of the control signal to the current source, and

current control circuitry for sensing a potential of the supply voltage at the supply voltage input port and for generating the control signal, where the control signal is for resulting in an increasing variable bias current with a decreasing supply voltage

sensed on the supply voltage input port which results in the second amplification stage to transition from a linear mode of operation to a saturation mode of operation.

18. A current source control circuit according to claim 17, comprising a supply voltage sensing circuit having a first input port for sensing of a potential of the supply voltage, a second input port for receiving a reference voltage and having an output port for providing a sense signal therefrom.

19. A current source control circuit according to claim 18 comprising a first multiplier circuit comprising at least a first input port connected to the supply voltage sense circuit for receiving the sense signal therefrom, a second input port for receiving a first reference current and having an output port for providing a first current therefrom.

20. A current source control circuit according to claim 19, wherein the first multiplier circuit comprises a Gilbert cell multiplier circuit.

21. A current source control circuit according to claim 19, comprising a bandgap current reference circuit having a first output port connected to the first multiplier circuit for providing the first reference current and a second output port for providing a second reference current.

22. A current source control circuit according to claim 21, comprising a current summing circuit having a first input port connected to the first multiplier circuit for receiving the first multiplier circuit output current therefrom, a second input port connected to bandgap current reference circuit for receiving the second reference current therefrom and an output port for providing a summed current therefrom, the summed current having a portion of the first current therein that is dependent upon the sense signal.

23. A current source control circuit according to claim 22, comprising

a second multiplier circuit comprising a first input port connected to the output port of the current summing circuit for receiving of the summed current, a second input port for receiving a ramp signal and an output port connected to the control signal output port for providing the control signal to the current source.

24. A current source control circuit according to claim 23, comprising:

an integrating capacitor; and,

a charge pump and ramp control circuit comprising an enable port for receiving of an enable signal, a first input port for connecting to the integrating capacitor and an output port for providing the ramp signal to the second multiplier circuit.

25. A current source control circuit according to claim 24, wherein the ramp signal comprises a rise time and a fall time, where both the rise time and the fall time are dependent upon a capacitance of the integrating capacitor.

26. A method of amplifying a RF input signal to form a RF output signal comprising the steps of:

sensing of a supply voltage potential;

determining whether the sensed supply voltage potential is one of higher than a first predetermined potential, in between the first predetermined potential and a second predetermined potential and below the second predetermined potential;

amplifying the RF input signal with a first amplification stage having a first variable gain to form a first amplified signal, the first variable gain dependent upon the sensed supply voltage potential;

amplifying the first amplified signal with a second amplification stage having a second gain to form the RF output signal;

adjusting a bias current provided to the first amplification stage for varying the first variable gain in such a manner that at the first predetermined potential a lower bias current is provided to the first amplification stage than is provided to the first amplification stage at the second predetermined potential, the lower bias current for operating of the second amplification stage in a linear mode of operation and a higher

bias current for operating of the second amplification stage in a saturation mode of operation.

27. A method according to claim 26, wherein between the first potential and the second potential the bias current provided to the first amplification increases with a decrease in the supply voltage potential.

28. A method according to claim 26, comprising the step of compensating for variability in the second gain of the second amplification stage in dependence upon the supply voltage variation by adjusting the bias current provided to the first amplification stage.

29. A method according to claim 26, wherein compensating for temperature variations is achieved by natural variations in the bias current in response to variations in temperature.

30. A method according to claim 27, wherein the bias current provided to the first amplification stage is additionally proportional to absolute temperature (PTAT).

31. A method according to claim 26, comprising the step of:

increasing of the bias current provided to the first amplification stage between the first predetermined potential and the second predetermined potential, the increasing in the bias current resulting in the second amplification stage to smoothly transition its mode of operation from the linear mode of operation to the saturation mode of operation.

32. A method according to claim 31, wherein the second gain of the second amplification stage is substantially fixed during the step of increasing of the bias current.